

NE253-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Katsuhiko Fukasaku

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the paragraphs beginning at page 7, lines 3-16 as follows:

FIGS. 1(A)-1(D) are process diagrams for showing a method for manufacturing an NMOSFET device according to a first embodiment of the present invention;

FIGS. 2(E)-2(H) are continued process diagrams for showing a method for manufacturing the NMOSFET device according to the first embodiment of the present invention;

FIGS. 3(I)-3(L) are further continued process diagrams for showing the method for manufacturing the NMOSFET device according to the first embodiment of the present

NE253-US

invention;

FIGS. 4(A)-4(D) are process diagrams for showing a method for manufacturing an NMOSFET device according to a second embodiment of the present invention;

FIGS. 5(A)-5(D) are process diagrams for showing a method for manufacturing a prior art NMOSFET device; and

REMARKS

The specification has been amended to indicate the identity of Figures 1(A)-1(D) through 5(A)-5(D).

Attached hereto is a marked-up version of the changes made to the specification by the current Amendment. The attached pages are captioned "**Version with markings to show changes made.**"

Early, favorable prosecution on the merits is respectfully requested.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please amend the paragraphs beginning at page 7, lines 3-16 as follows:

[FIG.1] FIGS. 1(A)-1(D) [is a process diagram] are process diagrams for showing a method for manufacturing an NMOSFET device according to a first embodiment of the present invention;

[FIG.2] FIGS. 2(E)-2(H) [is a continued process diagram] are continued process diagrams for showing a method for manufacturing the NMOSFET device according to the first embodiment of the present invention;

[FIG.3] FIGS. 3(I)-3(L) [is a further continued process diagram] are further continued process diagrams for showing the method for manufacturing the NMOSFET device according to the first embodiment of the present invention;

[FIG.4] FIGS. 4(A)-4(D) [is a process diagram] are process diagrams for showing a method for manufacturing an NMOSFET device according to a second embodiment of the present invention;

[FIG.5] FIGS. 5(A)-5(D) [is a process diagram] are process diagrams for showing a method for manufacturing a prior art NMOSFET device; and